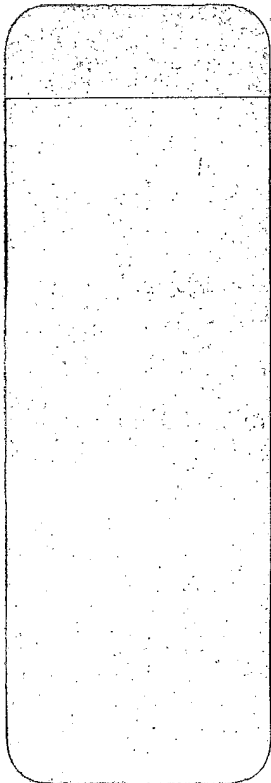


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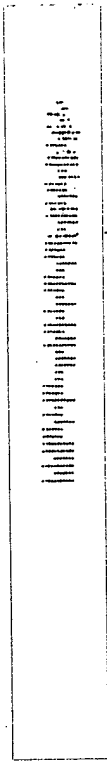
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/901,083	07/10/2001	Motoki Higashida	027260-477	7077

7590

08/11/2005

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Alexandria, VA 22313-1404

EXAMINER
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YANCHUS III, PAUL B

ART UNIT	PAPER NUMBER
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2116

DATE MAILED: 08/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

RECEIVED  
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AUG 26 2005

## Office Action Summary

Application No.

09/901,083

Applicant(s)

HIGASHIDA, MOTOKI

Examiner

Paul B. Yanchus

Art Unit

2116

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 27 May 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-12 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: \_\_\_\_\_

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### DETAILED ACTION

This non-final office action is in response to amendments filed on 5/24/05.

#### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-5, 7 and 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art [AAPA] in view of, Tobias et al., US Patent no. 6,363,501 [Tobias].

Regarding claim 1, AAPA teaches a leakage current reducing method of an LSI for reducing leakage current in an LSI chip divided into two parts; namely a main power supply region [main power supply region 18, Figure 7] including circuits operated by receiving power from a main power source [main power source 3, Figure 7], and a backup power supply region [backup power supply region 19, Figure 7] including a built-in storage section [built-in SRAM 15, Figure 7] for saving stored content [page 2, paragraph 3].

AAPA does not explicitly teach starting a scanning operation and reading information held in the memory units of each of the circuits provided in the main power supply region when the LSI chip is placed in an operation standby state.

Tobias also teaches a method of reducing power consumption of an LSI chip. Tobias teaches:

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connecting memory units [peripheral configuration registers, column 4, lines 19-25] in each of the circuits provided in the main power supply region through a scan path [SCAN\_PATH, column 4, lines 25-40];

starting a scanning operation, when the LSI chip is placed in an operation standby state [column 7, lines 22-35], through the scan path, and reading information [configuration data] held in the memory units of each of the circuits provided in the main power supply region [column 4, lines 36-40 and Figure 5]; and

saving the information thus read by the scanning operation [column 7, lines 1-9 and Figure 5].

It would have been obvious to one of ordinary skill in the art to combine the teachings of AAPA and Tobias. Utilizing a scan path to save information held in the memory units of each of the circuits provided in the main power supply region eliminates the need for the execution unit of the LSI to intervene when saving the information before placing the LSI chip into a standby state [Tobias, column 2, lines 52-60]. One of ordinary skill in the art would be motivated to modify the AAPA in view of Tobias because eliminating the need for the execution unit of the LSI to intervene when saving the information will reduce power consumption of the LSI.

AAPA and Tobias, as described above, teach using a scanning operation to save information of memory units before powering down a LSI in order to reduce leakage current. AAPA and Tobias do not specifically state that reading of the information during the scanning operation is based on a scan mode signal and a scanning clock pulse. However, Tobias does state that the scanning hardware is IEEE 1149.1 compliant [column 2, lines 52-60]. IEEE 1149.1 states that compliant scanning hardware must implement a test clock [TCK] and a test mode

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select [TMS] signals for controlling operations of the scanning hardware [pages 9-14].

Therefore, AAPA and Tobias do teach that the scanning operation is based on a scan mode signal and a scanning clock pulse.

Regarding claim 2, AAPA states that the built-in memory storage section is formed by SRAM [built-in SRAM 15, Figure 7 and page 2, paragraph 3].

Regarding claim 3, Tobias teaches saving the scanned information into a separate storage section [external memory 200, column 7, lines 1-9].

Regarding claim 4, AAPA states that the memory storage section is formed by SRAM [built-in SRAM 15, Figure 7 and page 2, paragraph 3].

Regarding claim 5, Tobias teaches using the JTAG boundary scan path to save configuration data to external memory [column 6, lines 47-63].

Regarding claim 7, AAPA states that the memory storage section is formed by SRAM [built-in SRAM 15, Figure 7 and page 2, paragraph 3].

Regarding claim 9, AAPA and Tobias do not specifically address presetting a voltage of the backup power source to be lower than a voltage of the main power source, yet enough for holding the content of the storage section provided in the backup power supply region. The examiner takes official notice that operating circuitry at a lower voltage level consumes a lower amount of power. Therefore, it would have been obvious to one of ordinary skill in the art to set the operating voltage of the backup power supply section to the lowest level which still permits the circuitry in the backup power supply region to successfully operate in order to save power in the LSI.

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Regarding claim 10, AAPA states that the built-in memory storage section is formed by SRAM [built-in SRAM 15, Figure 7 and page 2, paragraph 3].

Claims 6 and 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art [AAPA] and Tobias et al., US Patent no. 6,363,501 [Tobias], in view of, Goldstein, US Patent no. 6,684,275.

Regarding claim 6, Tobias teaches starting the scanning operation, when the LSI chip is placed in the standby state [column 7, lines 22-35], through the scan path, serially reading the information held in the memory units of each of the circuits provided in the main power supply region and saving the thus converted parallel information in specified addresses of the scanned information storage portion of the storage section [column 2, lines 23-27 and column 6, lines 47-55]; and

reading, when the LSI chip is returned from the standby state, the information held in the scanned information storage portion of the built-in storage section and setting the serial information through the scan path in the memory units of each of the circuits provided in the main power supply region [column 2, lines 23-27 and column 6, lines 47-55].

AAPA and Tobias do not explicitly teach converting the serial information into parallel information when storing the information into memory and converting the parallel information into serial information when reading the information from the memory. However, Goldstein states that serial/parallel conversion circuits are well known in the art to be used for converting a serial data stream to parallel in order to store the data in a memory and for converting parallel data to a serial data stream when reading the data from the memory [column 1, line 43 – column

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2, line 3]. It would have been obvious to one of ordinary skill in the art to convert the serial data to parallel data when storing the data in memory because parallel data is easier to store in memory [Goldstein, column 1, lines 50-58].

Regarding claims 11 and 12, AAPA, Tobias and Goldstein, as described above, teach a method for reducing leakage current in an LSI chip. Tobias also teaches saving the scanned information in an external storage [external memory 200, column 7, lines 1-9].

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art [AAPA] and Tobias et al., US Patent no. 6,363,501 [Tobias], in view of, Masabumi et al., JP-A 5-108194<sup>1</sup> [Masabumi].

AAPA and Tobias do not explicitly teach controlling the substrate bias voltage of transistors while the LSI is in a standby state. However, the Applicant's specification states that controlling the substrate bias voltage of transistors in a circuit to reduce the leakage current while in a standby state, as described in Masabumi, is a well-known concept [page 22, paragraph 1]. Therefore, it would have been obvious to one of ordinary skill in the art to employ the well-known method taught by Masabumi in the LSI taught by AAPA and Tobias in order to reduce the power consumption of the LSI when it is operating in a standby state.

### *Conclusion*

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

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<sup>1</sup> Included in IDS filed on 9/20/01

Art Unit: 2116

IEEE Standard Test Access Port and Boundary-Scan Architecture [IEEE 1149.1]

discloses a standard for test access port and boundary-scan hardware.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul B. Yanchus whose telephone number is (571) 272-3678. The examiner can normally be reached on Mon-Thurs 8:00-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H. Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul Yanchus  
August 4, 2005

  
**LYNNE H. BROWNE**  
**SUPERVISORY PATENT EXAMINER**  
**TECHNOLOGY CENTER 2100**

<b>Notice of References Cited</b>	Application/Control No. 09/901,083	Applicant(s)/Patent Under Reexamination HIGASHIDA, MOTOKI	
	Examiner Paul B. Yanchus	Art Unit 2116	Page 1 of 1

**U.S. PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-			
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
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**FOREIGN PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
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	Q					
	R					
	S					
	T					

**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	"IEEE Standard Test Access Port and Boundary-Scan Architecture", 1993, Institute of Electrical and Electronics Engineers, Inc., pages 9-14
	V	
	W	
	X	

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

# **IEEE Standard Test Access Port and Boundary-Scan Architecture**

Sponsor  
**Test Technology Standards Committee  
of the  
IEEE Computer Society**

Approved February 15, 1990  
**IEEE Standards Board**

Approved June 17, 1993  
**IEEE Standards Board**

**Abstract:** Circuitry that may be built into an integrated circuit to assist in the test, maintenance, and support of assembled printed circuit boards is defined. The circuitry includes a standard interface through which instructions and test data are communicated. A set of test features is defined, including a boundary-scan register, such that the component is able to respond to a minimum set of instructions designed to assist with testing of assembled printed circuit boards.

**Keywords:** boundary-scan, boundary-scan register, circuit boards, circuitry, printed circuit boards, test ports

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ISBN 1-55937-350-4

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## 2.4 References

The following publications shall be used in conjunction with this standard. When standards in this document are referred to, the latest revision shall apply.

[1] *JEDEC Publication 106-A*, Standard Manufacturer's Identification Code, The Joint Electron Device Engineering Council, July 1986.<sup>1</sup>

## 3. The Test Access Port (TAP)

The TAP is a general-purpose port that can provide access to many test support functions built into a component, including the test logic defined by this standard. It is composed as a minimum of the three input connections and one output connection required by the test logic defined by this standard. An optional fourth input connection provides for asynchronous initialization or the test logic defined by this standard.

### 3.1 Connections That Form the Test Access Port (TAP)

#### 3.1.1 Specifications

##### Rules

- a) The TAP shall include the following connections (defined in 3.3, 3.5, 3.6.2, and 3.7.2): TCK, TMS, TDI, and TDO.
- b) Where the TAP controller is not reset at power-up as a result of features built into the test logic, a TRST\* input shall be provided as defined in 3.8.2 (see also 5.3).
- c) All TAP inputs and outputs shall be dedicated connections to the component (i.e., the pins used shall not be used for any other purpose).

#### 3.1.2 Description

Dedicated TAP connections are required to allow access to the full range of mandatory features of this standard.

### 3.2 The Test Clock Input—TCK

TCK provides the clock for the test logic defined by this standard.

#### 3.2.1 Specifications

##### Rules

- a) Stored-state devices contained in the test logic shall retain their state indefinitely when the signal applied to TCK is stopped at 0.

##### Recommendations

- b) Since TCK inputs for many components may be controlled from a single driver, care should be taken to ensure that the load presented by TCK is as small as possible.

##### Permissions

- c) Stored-state devices contained in the test logic may retain their state indefinitely when the signal applied to TCK is stopped at 1.

<sup>1</sup>Copies can be obtained from JEDEC, 2001 I Street NW, Washington D.C. 20006, USA..

### 3.2.2 Description

The dedicated TCK input is included so that the serial test data path between components can be used independently of component-specific system clocks, which may vary significantly in frequency from one component to the next. It also permits shifting of test data concurrently with system operation of the component. The latter facility is required to support the use of the TAP and test data registers in a design for on-line system monitoring. The provision of an independent clock ensures that test data can be moved to or from a chip without changing the state of the on-chip system logic. The independent clock is also essential if boundary-scan registers are to be usable for board interconnect testing in all circumstances—including cases where system clock signals are derived in one component for use in others.

While TCK will in many cases be driven by a free-running clock with a nominal 50% duty cycle, there may be situations where the clock needs to stop for a period. One example is when an ATE needs to fetch test data from backup memory (e.g., disc), since some test systems are unable to keep the clock running during such an operation. This standard requires that TCK can be stopped at 0 indefinitely without causing any change to the state of the test logic. While the TCK signal is stopped at 0, stored-state devices are required to retain their state so that the test logic may continue its operation when clock operation restarts. Optionally, a component may also allow TCK to be stopped at 1 for an indefinite period.

Many parts of the test logic perform operations in response to the rising or falling edge of TCK, indicated by use of the phrase “on the rising (falling) edge of TCK.” These operations have to be completed within a fixed (frequency-independent) delay following the occurrence of the relevant change at TCK, and this delay has to be specified by the component supplier. Therefore, the phrase “on the rising (falling) edge of TCK” should be interpreted as “within a specified delay following the rising (falling) edge of TCK.”

NOTE — In many applications, the TCK signal applied to components that conform to this standard will have a duty cycle close to 50% (i.e., the periods that the clock spends at 0 and 1 will be equal). It is expected that all propagation delays will be such that correct operation is achieved under these circumstances, particularly when data is being transferred between TDO of one chip and TDI of another.

## 3.3 The Test Mode Select Input—TMS

The signal received at TMS is decoded by the TAP controller to control test operations.

### 3.3.1 Specifications

#### Rules

- a) The signal presented at TMS shall be sampled by the test logic on the rising edge of TCK.
- b) The design of the circuitry fed from TMS shall be such that an undriven input produces a response identical to the application of a logic 1.

#### Recommendations

- c) Since the TMS inputs for many components may be controlled from a single driver, care should be taken to ensure that the load presented by TMS is as small as possible.

### 3.3.2 Description

Rule 3.3.1b is included so that the TAP controller is forced into the *Test-Logic-Reset* controller state in the case of an undriven TMS pin. This ensures that normal operation of the complete design can continue without interference from the test logic (see 6.2). For TTL-compatible designs, the rule may be met by including a pull-up resistor in the component's TMS input circuitry.

Signal values presented at TMS are sampled by the test logic on the rising edge of TCK. It is expected that the bus master (ATE, bus controller, etc.) will change the signal driven to the TMS inputs of connected components on the falling edge of TCK. The waveforms shown elsewhere in this standard reflect this expectation.

### 3.4 The Test Data Input—TDI

Serial test instructions and data are received by the test logic at TDI.

#### 3.4.1 Specifications

##### Rules

- a) The signal presented at TDI shall be sampled into the test logic on the rising edge of TCK.
- b) The design of the circuitry fed from TDI shall be such that an undriven input produces a response identical to the application of a logic 1.
- c) When data is being shifted from TDI towards TDO, test data received at TDI shall appear without inversion at TDO following a number of rising and falling edges of TCK determined by the length of the instruction or test data register selected.

#### 3.4.2 Description

The data pins (TDI and TDO) provide for serial movement of test data through the circuit. The requirement for data to be propagated from TDI to TDO without inversion is included to simplify the operation of components compatible with this standard linked on a printed circuit board.

Values presented at TDI are clocked into the selected register (instruction or test data) on a rising edge of TCK. It is expected that the bus master (ATE, bus controller, etc.) will change the signal driven to the TDI input of the first component on a serial board-level path on the falling edge of TCK. The waveforms shown elsewhere in this standard reflect this expectation.

Rule 3.4.1b is included so that open-circuit faults in the board-level serial test data path cause a defined logic value to be shifted into the test logic. Note that when this constant value is shifted into the instruction register the bypass register will be selected (as will be discussed further in 7.4). For TTL-compatible designs, this rule may be met by inclusion of a pull-up resistor in the component's TDI input circuitry.

### 3.5 The Test Data Output—TDO

TDO is the serial output for test instructions and data from the test logic defined in this standard.

#### 3.5.1 Specifications

##### Rules

- a) Changes in the state of the signal driven through TDO shall occur only on the falling edge of TCK.
- b) The TDO driver shall be set to its inactive drive state except when the scanning of data is in progress (see 5.2).

#### 3.5.2 Description

To ensure race-free operation, changes on TAP inputs (TMS and TDI) are clocked into the test logic defined by this standard on the rising edge of TCK while changes at the TAP output (TDO) occur on the falling edge of TCK. Similarly, for test logic able to drive or receive signals from system pins (e.g., the boundary-scan register), signals driven out of the component from the test logic change state on the falling edge of TCK, while those entering the test logic are clocked in on the rising edge (as will be discussed in 8.3).

The contents of the selected register (instruction or data) are shifted out of TDO on the falling edge of TCK. In the illustrations given in this document, edge-operated circuit designs are generally used. For an edge-operated implementation, note that the TDO output changes shall be delayed until the falling edge of TCK, which can be achieved by including a flip-flop clocked by the falling edge of TCK in the TDO output buffer. Where the registers are constructed from master and slave latches controlled by non-overlapping clocks, the retiming required by rule 3.5.1a is an inherent feature of the design.

The capability of TDO to switch between active and inactive drive is required to allow parallel, rather than serial, connection of board-level test data paths in cases where this is required. In TTL or CMOS technologies, for example, this requirement may be met through use of a 3-state output buffer.

### 3.6 The Test Reset Input—TRST\*

The optional TRST\* input provides for asynchronous initialization of the TAP controller (see 5.3).

#### 3.6.1 Specifications

##### Rules

- a) If TRST\* is included in the TAP, then the TAP controller shall be asynchronously reset to the *Test-Logic-Reset* controller state when a logic 0 is applied to TRST\* (see 5.3).  
NOTE — As a result of this event, all other test logic in the component is asynchronously reset to the state required in the *Test-Logic-Reset* controller state.
- b) If TRST\* is included in the TAP, then the design of the circuitry fed from that input shall be such that an undriven input produces a response identical to the application of a logic 1.
- c) TRST\* shall not be used to initialize any system logic within the component.

##### Recommendations

- d) To ensure deterministic operation of the test logic, TMS should be held at 1 while the signal applied at TRST\* changes from 0 to 1.

#### 3.6.2 Description

Initialization of the TAP controller in turn causes asynchronous initialization of other test logic included in the design, as discussed in the subsequent chapters of this standard.

Rule 3.6.1b is included to ensure that, in the case of an unterminated TRST\* input, test logic operation can proceed under control of signals applied at the TMS and TCK inputs. For TTL-compatible designs, this rule may be met by inclusion of a pull-up resistor in the TRST\* input circuitry of the component.

Rule 3.6.1c ensures that the test logic can be reset independently of the on-chip system logic. This allows the test logic to be disabled by hard-wiring TRST\* to logic 0.

Recommendation 3.6.1d is included to ensure that the test logic responds predictably when the signal applied to TRST\* changes from 0 to 1. If rising edges occur simultaneously at TRST\* and TCK when a logic 0 is applied to TMS, a race will occur, and the TAP controller may either remain in the *Test-Logic-Reset* controller state or enter the *Run-Test/Idle* controller state.

### 3.7 Interconnection of Components Compatible With This Standard

#### 3.7.1 Specifications

##### Permissions

- a) The TAP input and output connections may be interconnected at the board level in a manner appropriate to the assembled product.

#### 3.7.2 Description

Figures 3-1, 3-2, and 3-3 illustrate three alternative board-level interconnections of components conforming to this standard.

In each example, the test bus may be controlled either by an ATE system or by a component that provides an interface to a test bus at the next level of product assembly (for example, at the board/backplane interface). In this standard, the device that controls the board-level test bus is referred to as the bus master.

Note that the minimum configuration (shown in figure 3-1) contains:

- a) Two broadcast signals (TMS and TCK) fed from the testability bus master to all slaves in parallel;
- b) A serial path formed by a daisy-chain connection of the serial test data pins (TDI and TDO).

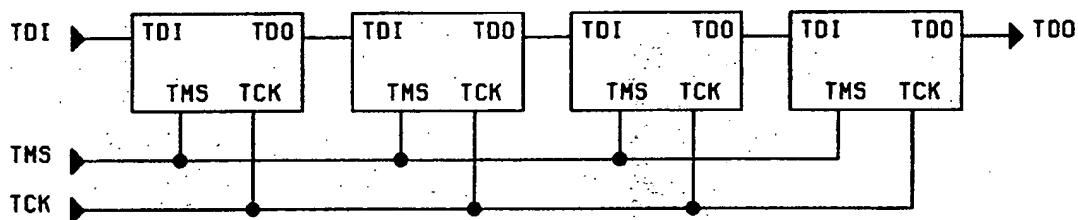


Figure 3-1—Serial Connection Using One TMS Signal

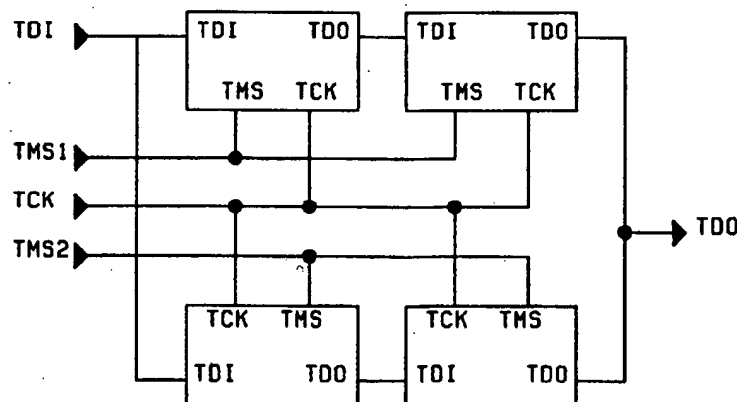


Figure 3-2—Connection in Two Paralleled Serial Chains

The hybrid serial/parallel connection shown in figure 3-2 uses a pair of coordinated TMS signals (TMS1 and TMS2) to ensure that only one serial path is scanning data at a given time. This configuration makes use of the 3-state feature of the TDO output pin, which ensures that only the components that are scanning data have TDO in the active drive state.

Figure 3-3 shows the four components connected to give four separate serial paths through the complete board design. These paths have separate TDI and TDO signals, but can be controlled from common TCK and TMS signals.

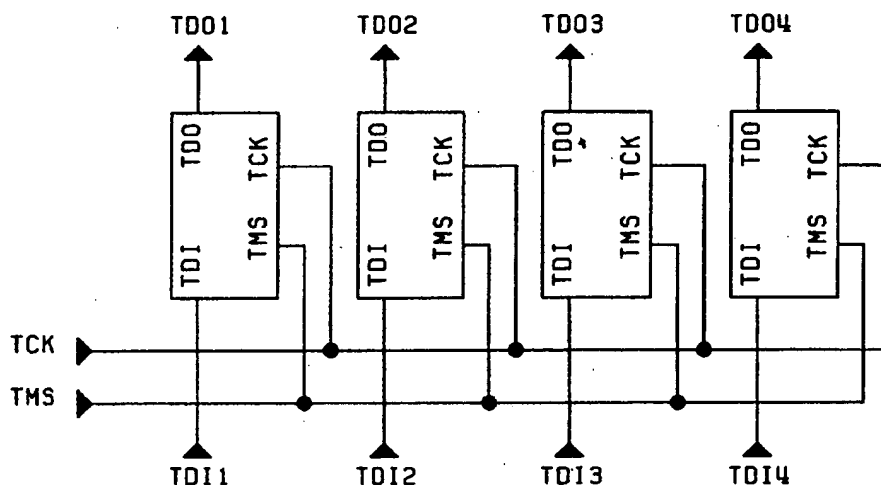


Figure 3-3—Multiple Independent Paths With Common TMS and TCK Signals

### 3.8 Subordination of This Standard Within a Higher Level Test Strategy

While the test logic specified by this standard has been designed to be extensible to meet the particular needs of individual designers or companies (for example, by the flexibility of the instruction register), occasions may arise when it will be desirable to terminate compliance with this standard by a component temporarily and enable complementary test functionality. An example (illustrated in the Appendix) involves a Level-Sensitive Scan Design (LSSD) infrastructure required for use during “stand-alone” component testing, which cannot be simultaneously operated with the test functionality defined by this standard (which is required to support testing of boards onto which the components implementing the two testing techniques will be assembled.)

This clause defines how compliance with this standard may be “switched on” or “switched off.” The rules require the change of test functionality to be under the control of signals applied at one or more component pins. Compliance has to be effected by a single logic pattern applied at these pins, and not by a sequence of such patterns.

## **NEW CENTRAL FAX NUMBER**

Effective July 15, 2005

On July 15, 2005, the Central FAX Number will change to **571-273-8300**. This new Central FAX Number is the result of relocating the Central FAX server to the Office's Alexandria, Virginia campus.

Most facsimile-transmitted patent application related correspondence is required to be sent to the Central FAX Number. To give customers time to adjust to the new Central FAX Number, faxes sent to the old number (703-872-9306) will be routed to the new number until September 15, 2005. After September 15, 2005, the old number will no longer be in service and **571-273-8300** will be the only facsimile number recognized for "centralized delivery".

**CENTRALIZED DELIVERY POLICY:** For patent related correspondence, hand carry deliveries must be made to the Customer Service Window (now located at the Randolph Building, 401 Dulany Street, Alexandria, VA 22314), and facsimile transmissions must be sent to the Central FAX number, unless an exception applies. For example, if the examiner has rejected claims in a regular U.S. patent application, and the reply to the examiner's Office action is desired to be transmitted by facsimile rather than mailed, the reply must be sent to the Central FAX Number.